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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,961	09/26/2003	Glenn J. Leedy	ELM-2 CONT. 4	9439

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EXAMINER	
LEWIS, MONICA	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,961	LEEDY, GLENN J.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *30days* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *88-115* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *88-115* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This restriction is in response to the amendment filed September 26, 2003.

Election/Restrictions

2. This application contains claims directed to the following patentably distinct species of the claimed invention:

Embodiment I (Claims 88-94 and 115), directed to a semiconductor component, first substrate, a second substrate bonded to the first to form conductive paths, a second substrate that is thinned and has one of active and passive circuitry formed thereon;

Embodiment II (Claims 88, 95-98 and 102), directed to a semiconductor component, first substrate, a second substrate bonded to the first to form conductive paths and having circuitry formed thereon, at least one additional thinned substrate having circuitry formed thereon bonded to one of the second substrate or an adjacent additional thinned substrate and wherein at least two of the first, the second and the at least one thinned substrates are formed using a different process technology, the second and the at least one additional thinned substrates comprises a microprocessor and at least one of the substrate of the first, the second and the at least one additional thinned substrates has memory circuitry, at least one of the substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs tests on the at least substrate that has memory circuitry formed thereon;

Embodiment III (Claims 88, 95 and 99), directed to a semiconductor component, first substrate, a second substrate bonded to the first to form conductive paths and having circuitry formed thereon, at least one additional thinned substrate having circuitry formed thereon bonded to one of the second substrate or an adjacent additional thinned substrate, at least one of the substrate of the first, the second and the at least one additional thinned substrates has memory circuitry, the memory circuitry having a plurality of memory locations, wherein at least one memory location of the plurality is used for sparing and wherein data from the at least one memory location is used instead of data from a defective memory location;

Embodiment IV (Claims 88, 95, 100 and 104), directed to a semiconductor component, first substrate, a second substrate bonded to the first to form conductive paths and having circuitry formed thereon, at least one additional thinned substrate having circuitry formed thereon bonded to one of the second substrate or an adjacent additional thinned substrate, at least one of the substrate of the first, the second and the at least one additional thinned substrates has memory circuitry, at least one of the substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs programmable gate line address assignment with respect to the at least one substrate that has memory circuitry formed thereon;

Embodiment V (Claims 88, 95 and 101), directed to a semiconductor component, first substrate, a second substrate bonded to the first to form conductive paths and

having circuitry formed thereon, at least one additional thinned substrate having circuitry formed thereon bonded to one of the second substrate or an adjacent additional thinned substrate, wherein information processing is performed on data routed between the circuitry of at least two of the first, the second and the at least one additional thinned substrates, a plurality of vertical interconnections that traverse at least one of the first, the second and the at least one additional thinned substrate;

Embodiment VI (Claims 88, 95 and 103), directed to a semiconductor component, first substrate, a second substrate bonded to the first to form conductive paths and having circuitry formed thereon, at least one additional thinned substrate having circuitry formed thereon bonded to one of the second substrate or an adjacent additional thinned substrate, wherein information processing is performed on data routed between the circuitry of at least two of the first, the second and the at least one additional thinned substrates and at least one additional thinned substrates has reconfiguration circuitry;

Embodiment VII (Claims 88, 95 and 105), directed to a semiconductor component, first substrate, a second substrate bonded to the first to form conductive paths and having circuitry formed thereon, at least one additional thinned substrate having circuitry formed thereon bonded to one of the second substrate or an adjacent additional thinned substrate, a memory array, circuitry that generates a gate control signal and a controller; and

Embodiment VIII (Claims 88, 95, 106-114), directed to a semiconductor component, first substrate, a second substrate bonded to the first to form conductive paths and having circuitry formed thereon, at least one additional thinned substrate having circuitry formed thereon bonded to one of the second substrate or an adjacent additional thinned substrate, a controller substrate, a memory substrate, a plurality of data lines, a plurality of gate lines, an array of memory cells, a gate line selection circuit, a controller substrate logic that tests the array of memory cells and removes references in the address assignments to gate lines.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claim 88 is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

3. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee under 37 CFR 1.17(i).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

April 13, 2005

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